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Active Learning Techniques in Digital Design Education for Engineering Technology Students

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RESEARCH PAPER

Abstract

The goal of this paper is to describe the motivation, methodology and results of introducing Active Learning Techniques in a Digital Design course. Digital Design is a four-credit junior level course for electrical and computer-engineering technology majors at Farmingdale State College, State University of New York. The students enrolled in this course have a large range of skills in term of experience with laboratory equipment, computer-based tools, and programming. The course introduces students to VHDL Hardware Description Language as the design entry method for digital circuits and to Field Programmable Gate Arrays (FPGA) platforms for the implementation of the digital circuits. Active learning techniques implemented in the course offer students more learning opportunities, potentially improving students' knowledge and skills in digital design.

Keywords: Active Learning, Digital Design, VHDL, Flipped Classroom

Related ASEE Publications

M. Radu, "Applying the Flipped Classroom Pedagogy in a Digital Design," in Proceedings of the 2019 national ASEE Conference, 2019.

1 Introduction

In traditional approaches to teaching engineering classes, the instructor plays the role of information conveyor while the students assume a receiver role with primary responsibilities of listening and note taking. Research suggests that students need to be more actively engaged with course material to maximize their understanding [1]. Research has supported that active learning strategies result in higher student engagement and greater learning gains as compared to traditional instructor-centered methods such as lecture [1–3].

Introducing active learning techniques in digital design education for electrical and computer engineering technology students is aligned with the College Mission to be recognized as a center of excellence in teaching and applied learning, by creating a distinctive identity in preparing students as highly qualified professionals through expanding mentoring, research, and experiential learning [4].

This paper focuses on two learning active techniques: Flipped Classroom and Project-Based-Learning. The Flipped Classroom is a pedagogical model that reverses the typical lecture and homework components of the course. The content-heavy lecture is usually replaced by computer-based individual instruction – such as online videos – and face-to-face classroom time is spent on interactive group learning activities, discussion of difficult concepts and problem solving [5]. Project-Based-Learning is an instructional method that challenges students to think critically and enhance their ability to analyze and solve real world problems, develop skill in gathering and evaluating information needed for solving problems, gain experience working cooperatively in

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teams and small groups, and acquire versatile and effective communication skills [6, 7]. Project-Based-Learning motivates students by engaging them in their own learning. The traditional teacher and student roles change: the student assumes increasing responsibility for their learning, setting a pattern to become successful life-long learners, and the teacher becomes a resource, tutor, and evaluator, guiding them in their problem solving efforts. Project-Based learning helps make learning relevant and useful to students by establishing connections to life outside the classroom, addressing real world concerns, and developing real world skills [6].

This paper summarizes the process of implementing active learning techniques in a digital design course and presents the results, including assessment data. The target course is EET 316 - Digital Design. This course is a four-credit junior-level course for electrical and computer-engineering technology majors at Farmingdale State College. The students enrolled in this course have a large range of skills in term of experience with laboratory equipment, computer-based-tools, programming and communication skills. Transfer students from community colleges located in Long Island and New York metropolitan area represents approximately 40 % of the class. Some of the challenges that the students are facing in this course are: (i) mastering fundamental digital circuits such as multiplexers, decoders, registers, counters, covered in prerequisite courses; (ii) writing VHDL code describing these fundamental digital circuits following specific templates; (iii) properly performing functional verification (writing test benches following templates and applying to a specific circuit; (iv) efficiently using computer-based design tools to design, simulate and implement digital circuits. To address these problems, the author of this paper introduces various active learning techniques that offer students more "hands-on" learning opportunities (experiential learning), potentially improving students' knowledge and skills in digital design.

The remainder of this paper is organized as follows: Section II presents similar work. Section III presents the characteristics of student population at Farmingdale State College. Section IV presents the Digital Design sequence of courses. Section V presents the methodology. Section VI presents results. Section VII concludes the paper.

2 Similar Work

Being considered high impact active learning practices, Flipped Classroom and Project-Based-Learning (PBL) are routinely implemented in undergraduate and graduate level courses in all STEM fields. The majority of the papers presents active learning techniques for four years engineering programs, such as electrical and computer engineering, chemical engineering, civil engineering, etc., but few papers present "flipped" courses and PBL for engineering technology programs.

While there is overwhelming evidence provided by literature for the added benefit of the Flipping Classroom concept, the majority of the surveyed papers present examples of full "flipped" courses, not just specific course modules, as presented in this paper. Cronhjort and Weurlander [8] used "focus group interviews and the student perspective in order to investigate student perceptions of flipped classroom in engineering education in many courses and subjects. The perceived advantages, strengths, drawbacks, or difficulties, and students' views on learning with flipped classroom were investigated". Bachnak and Maldonano [9] presents how a flipped classroom technique was incorporated into a three-credit electrical engineering course. The paper discusses "student survey results, and describes plans to improve the delivery of this and similar courses". Tomas and Salvador [10] focuses on the implementation, development, documentation, analysis, and assessment of the flipped classroom methodology, for a pilot group of chemical and materials engineering undergraduate students. "Results show that this technique promotes self-learning, autonomy, time management as well as an increase in the effectiveness of classroom hours". Rafla and Jacinto [11] presents the lessons learned from flipping the classroom of an entry-level graduate course on digital hardware design. The course covers hardware description languages (HDLs) and requires students to successfully design, simulate, synthesize, and verify digital circuits using hands-on projects and in-class activities. It is important to note that the authors of this papers notice, "typically students struggle with provided in-class activities, assignments, and projects in any digital hardware design class". The authors conclude that "from an instructional perspective,

regardless of drawbacks, the new active-learning environment and teaching techniques allowed for the instructor to reinforce and delve deeper into course content while allowing students to work efficiently with new material. Ayala, Popescu and Jovanovic [12] discusses the implementation of the Flipped Classroom method in a Fluid Mechanics course in an Engineering Technology program. "A survey was distributed to the students at the end of the course as a post-class activity, concluding the implementation considered in the study. The results of the survey showed that the students were satisfied with the teaching method and found it important in their learning process".

Project-Based-Learning (PBL) is introduced in a large number of undergraduate and graduate courses, ranging from one course or a sequence of course to an entire curriculum. The PBL presented in this paper is introduced in the last weeks of the semester, both theory and lab sessions. Kruse, Feng and Curtis [13] presents a real-world project that was implemented in a Computer-Aided Design (CAD) product design class. "This active project-based learning experience and curriculum design allows students to see beyond textbook examples and permits them to build a strong foundation in communication skills, engineering design, project implementation, project analysis and assessment". Sameer, Fini, Mellat and Sarin [14] discusses the results of a study on the effect of project-based learning (PBL) on students' learning outcomes in a Transportation Engineering required junior level course in a Civil Engineering curriculum. The course was transformed from a lecture-based course to a project-based course, integrating a semester-long project as a stimulus for students' learning. "The results show that the use of the project-based approach significantly improved students' ease of learning the subject matter". Northern and Fuller [6] presents PBL applied to Digital Circuits and Design Sequence (DCDS) courses with the intent to help prepare electrical and computer engineering students for industry or research through application-driven exercises. The goal of the DCDS is to improve student learning of theoretical concepts in digital circuitry through project-based learning exercises using an FPGA platform for rapid prototyping of complex designs. Stone and Jack [15] outlines a unique approach, a shared PBL course sequence for engineering and technology engineering students. The teams contain a multidisciplinary mix of students with a range of practical and theoretical approaches. "PBL instructors embrace this diversity and foster an environment that is much more productive and capable that a single program experience could offer". Ulseth and Johnson [16] presents the "Iron Range" PBL for graduates of Minnesota's community colleges. Unique attributes of the program include "industry clients, semester-long projects, dedicated project rooms, technical competence learned in one-credit, small (3-4 student) groups with one academic staff called learning competencies, and an emphasis on continuous improvement".

3 Characteristics of Student Population at Farmingdale State College

The active learning techniques presented in this paper were designed for students enrolled in the Electrical and Computer Engineering Technology program at Farmingdale State College. The Department of Electrical and Computer Engineering Technology attracts a large number of transfer students from community colleges located in Long Island and New York metropolitan area. Offering Bachelor of Science degrees in Engineering Technology, the program mainly focuses on hands-on skills. The BS in Engineering Technology and BS in Engineering degree programs are closely related but have noticeable differences in learning curriculum. The BS in Engineering emphasizes theories and advanced concepts, while a BS in Engineering Technology emphasizes hands-on application and implementation [17].

The general characteristics of student population at Farmingdale State College were also taken into consideration.

A study of student population at FSC shows the following: over 90 % of the students are commuting on daily basis from the greater New York metropolitan area and they hold full time jobs; around 35% are first-generation college students (e.g., neither parent has earned a 4-year degree); 30% are minority; the student population includes a large number of "New Americans" (i.e., they or their parents were born outside of the US); and many students have considerable financial need (30% receiving Pell grants) [18]. The study concludes: "to educate today's new undergraduate

student effectively, one needs to engage students in active, experiential learning," which is the focus of this paper.

4 Description of Digital Design Sequence of Courses

The digital design education in the Department of Electrical and Computer Engineering Technology at Farmingdale State College is accomplished by a sequence of three courses: EET 105-Introduction to Digital Electronics, EET 223-Digital Electronics and EET 316-Digital Design. Each course is taught by various instructors, both from academia and industry. The first digital course in the sequence, Introduction to Digital Electronics, presents fundamental concepts of digital electronics, specifically combinational logic circuits. The second course, Digital Electronics, reinforces the analysis and design of combinational and introduces sequential logic circuits. The third course, Digital Design, introduces students to more advanced concepts in digital design.

EET 316-Digital Design is a four-credit junior level course (theory-3 credits, lab-1 credit). The course introduces students to VHDL Hardware Description Language as the design entry method and to Field Programmable Gate Arrays (FPGA) platforms for the implementation of digital circuits, using Xilinx design tools. After taking this course students should be able to: (i) design and analyze combinational and sequential logic circuits; (ii) trace the behavior of digital circuits by completing and analyzing timing diagrams. (iii) Use VHDL and Schematic Capture to design, simulate, and implement digital circuits; (iv) Draw a state diagram and implement solution to a digital design using Finite State Machine based controller.

In the last seven years, EET 316-Digital Design was updated continuously and active learning pedagogies were incorporated. The changes were made by the author of this paper, who was appointed course coordinator in the Fall of 2014. The platforms used for the lab experiments are based on Xilinx FPGA chip and manufactured by DigilentInc [17, 19]. In the academic year 2013-2014 a new lab manual was created, teaching students design entry (Schematics and VHDL) using Xilinx ISE tools and Digilent ADEPT software. In the academic year 2014-2015 the lab manual was updated, adding more experiments, but no changes were made to the theory class, compared with the previous academic year. In the academic year 2015-2016 changes were made to the course topics based on instructor's observations and students' very strong feedback. The VHDL language was introduced earlier in the semester. New concepts such as clock skew and meta-stability of digital circuits were introduced. In the academic year 2016-2017 the lab manual was updated again, incorporating more complex labs covering VHDL and Functional Verification (Test Benches). In the academic year 2017-2018 the Flipped Classroom pedagogy was introduced, followed by Project Based Learning in the academic year 2018-2019. In the academic year 2019-2020, a set of active learning modules were developed around the Analog Discovery platform, with the primary objective to enhance students learning by increasing their "hands-on" experience in building and debugging digital circuits. The Analog Discovery platform developed by DigilentInc provided a simple tool for students to build and test real-world functional circuits, perform experiments, run simulations and troubleshoot. As an alternate lab, it took the place of expensive laboratory equipment such as function generators and oscilloscope, making this platform affordable, portable, and accessible to students anytime, anywhere. Due to the Covid-19 pandemic some of the envisioned changes were delayed to the Fall semester 2021. The Flipped Classroom and PBL are described in detail in Section V of the paper. Appendix I presents the syllabus of the course and the current sequence of lab experiments.

To better prepare students for the Digital Design course, the following active learning techniques were introduced in EET 105-Introduction to Digital Electronics and EET 223-Digital Electronics courses (prerequisites). For EET 105-Introduction to Digital Electronics course a set of basic experiments were created around the Analog Discovery platform, allowing students to work at home, at their own pace. The experiments were created to help students improve their debugging skills and to become proficient using test equipment outside the traditional laboratory settings [20]. The experiments and associated tutorials were made available to students through BlackBoard. For EET 223-Digital Electronics Lab, a small project module was developed. The Digital Clock

project was offered for the first time to the students enrolled in this course in the academic year 2016-2017.

5 Methodology

In the academic year 2017-2018 the Flipped Classroom pedagogy was introduced. The following topics (modules) were identified to benefit mainly from the flipped classroom pedagogy.

- **Description and functional verification of combinational circuits using VHDL**
- **Description and functional verification of sequential circuits using VHDL**
- **Description and functional verification of Finite State Machine using VHDL**

In the traditional Digital Design course, prior to Fall 2017, description and functional verification of digital circuits using VHDL were covered using PowerPoint slides. All the lectures were posted online at the beginning of each semester, allowing students to access them before the class (available on BlackBoard). For the Flipped Classroom, the existing Power Point lectures were converted into Panopto video lectures, with support from the instructional support specialists. The intention was to record the PowerPoint slides and on-screen content along with audio of the instructor presenting. The flipped classroom modules were created and were added to the EET 316 course content on Blackboard, as seen in Figure 1.

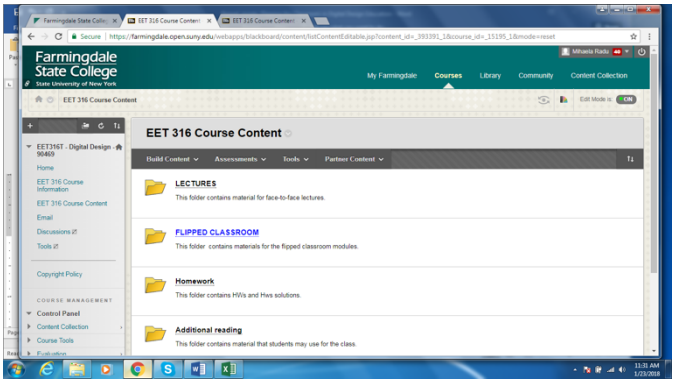

Figure 1. EET 316 course content

The flipped classroom folder has three separate modules, one for each topic, as seen in Figure 2.

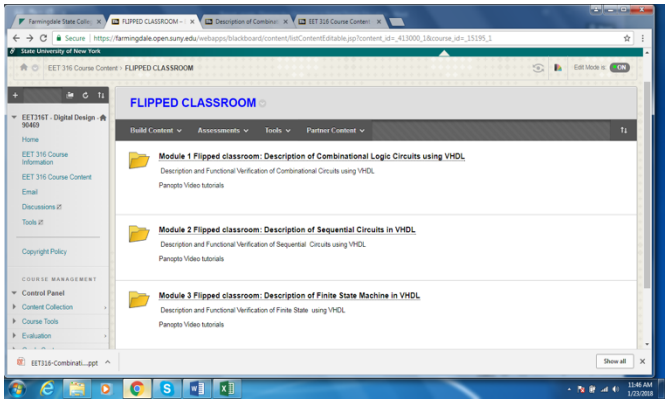

Figure 2. Flipped Classroom Content

Out of class activities: Before the class, students are tasked to listen to the audio tutorials and come to class prepared. They are provided with adequate information before every flipped classroom module. Figure 3 presents the Panopto tutorial for description of combinational circuits using VHDL.

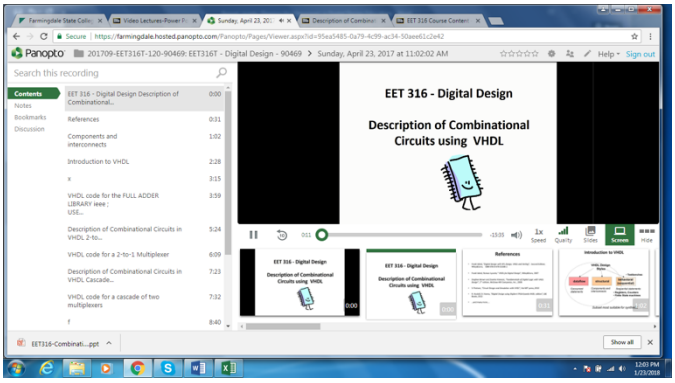

Figure 3. Example of Panopto tutorial –Description of Combinational Circuits using VHDL

In class activities: At the beginning of the class, students receive a 5-minute quiz regarding the content of the Panopto tutorial. Students are asked to fill the statement with the appropriate word(s): "Sequential statements can only be used inside of a _____ block." or, "In a test bench for sequential circuits, give ____ value to the signal CLK at the moment t_0=0 ns."

The instructor briefly covers the PP slides, reinforces key concepts and answers students' questions. Figure 4 presents the organization of in-class activities for one of the "flipped" modules. It contains quizzes, in-class assignments and tutorials for using Xilinx tools. The existing tutorials regarding the use of Xilinx design tool (currently available on BlackBoard for use in the lab) were updated for use during the theory class.

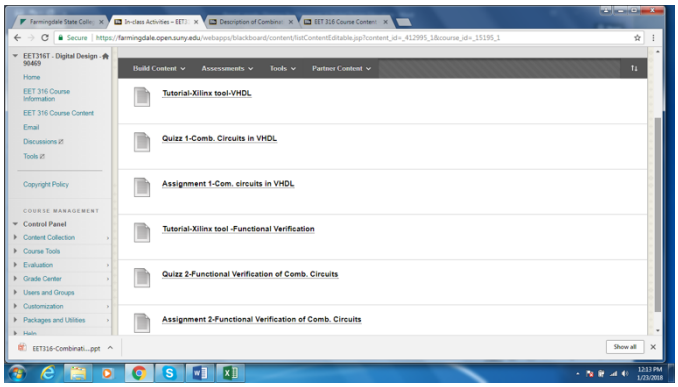

Figure 4. In class Activities for a Flipped Classroom Module

Throughout almost the entire class period, students engage in activities specific to digital design: **Design Entry** (using VHDL language) and Design Synthesis (translation of VHDL into an industry standard format) using Xilinx design tools. Students design digital circuits following examples ("VHDL templates") provided in the notes posted online. They perform also functional verification of the circuits, by writing and applying test benches to the circuits and analyzing resulting waveforms. Students work individually but they are allowed to communicate with each other and share results.

By implementing these hands-on activities during the class, students are better prepared for laboratory experiments and more time can be dedicated to the implementation processes of complex logic circuits: **Design Implementation** (translate, map, place and route) and **Device Programming** (generate a configuration file and download on the FPGA platform). In the previous traditional approach (without Flipped Classroom) students performed all the steps of the design during three laboratory hours, which proved sometimes insufficient. Sometimes students struggle to finish the activities in the dedicated time and often wind up missing important concepts in an effort to complete the lab. The planned in-class activities during theory course have the potential to improve students' problem-solving skills, analytical and critical skills, which are essentials in the

engineering field.

The implementation of the Flipped Classroom pedagogy and the previous changes in the Digital Design course “paved the way” to introduce the Project-Based-Learning pedagogy.

In the academic year 2018-2019, Project-Based-Learning was introduced. In the last two-three weeks of the semester, after introducing the FSM concept in the theory class, each student was tasked to design and implement a Vending Machine controller using VHDL language and FPGA platforms, being given written specifications and the state diagram of the Finite State Machine (controller). Students had to identify inputs, outputs, states and transitions of the state diagram, assign proper inputs to switches and outputs to LEDs on the FPGA board, etc. Students were tasked to perform a detailed functional verification by writing test benches, generating waveforms, analyzing and interpreting the results: does the machine cycle thorough all states, are the right outputs generated, is the reset signal activated properly? Students had to demonstrate their projects to the lab instructor before submitting detailed lab reports. The introduction of the project is supported by the previous twelve lab experiments. The lab introducing the use of the Clock Divider (Slow Clock) and Seven Segment Display are incorporated in the project design. Figure 5 presents the state diagram of the vending machine controller, while Figure 6 presents the actual implementation and testing of the Vending Machine.

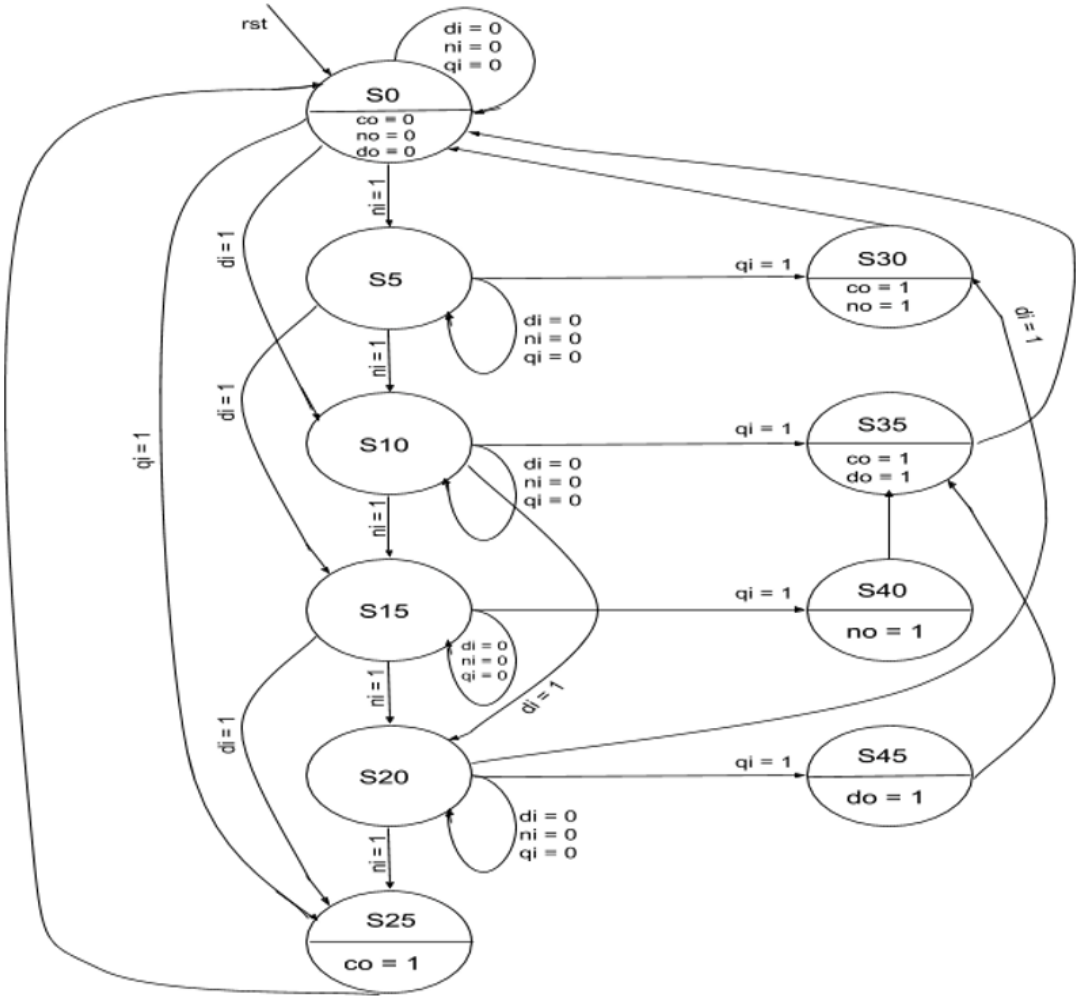

Figure 5. Vending Machine State Diagram

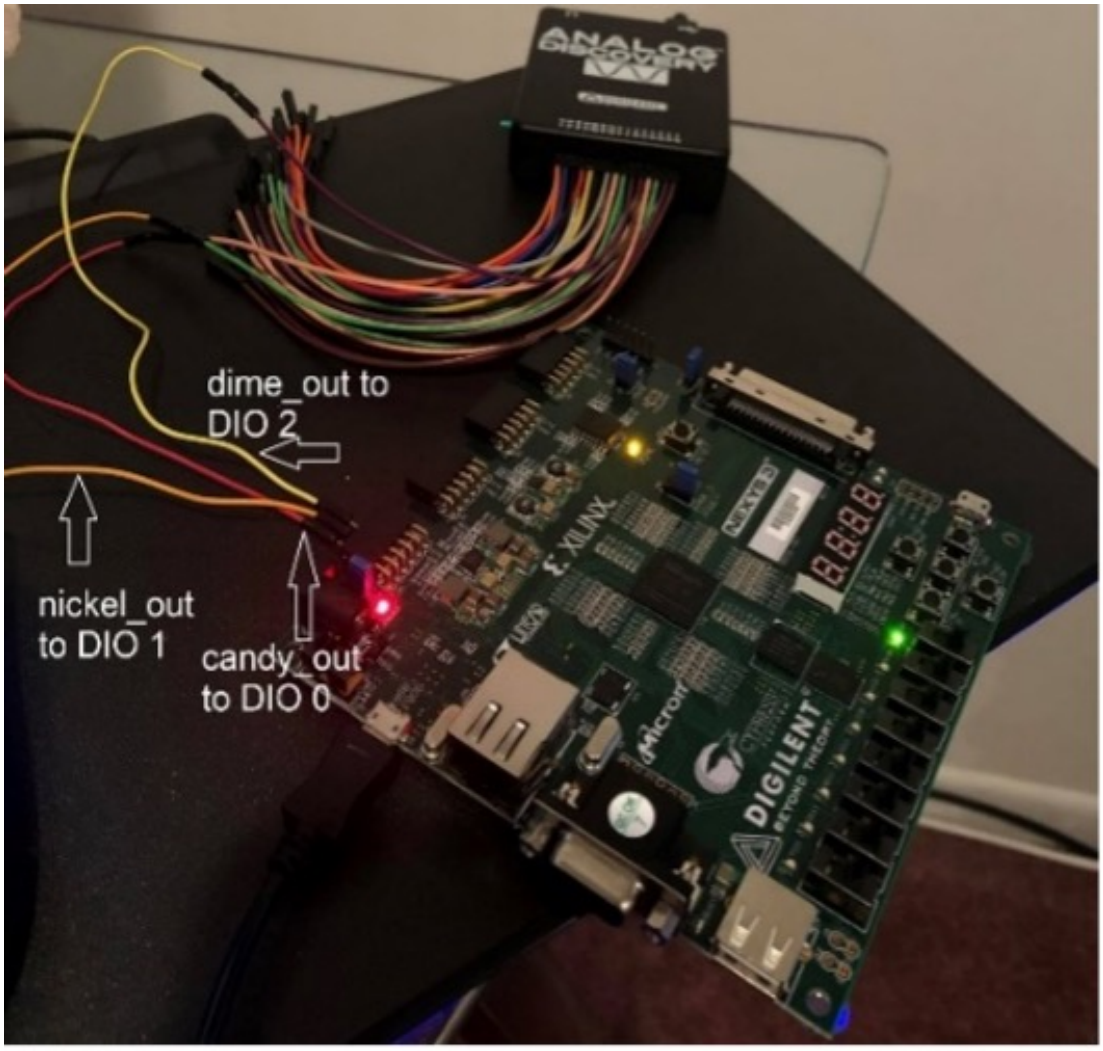

Figure 6. Vending Machine Implementation

6 Results

Only the courses and the associated labs that were taught by the same instructor were considered for the assessment. An IRB (Institutional Review Board) protocol was secured for the Project Based Learning concept, allowing to present baseline data starting Fall 2017.

Student knowledge was assessed from answers to selected questions of the final exam, related to course objectives. The goal for the course is that 70% of students meet the course assessment standard, which states that an overall score over 84% exceeds the standard, an overall score between 70 % and 84 % meets the standard, an overall score between 60% and 69% approaches the standard, while an overall score below 60 % does not meet the standard, according to ABET accreditation for the EET department.

Table 1 presents students' final exam scores from Fall 2017 to Fall 2019 semesters (including min, max scores and standard deviation) and the average scores for two questions. All the exams are open notes, books, etc. The questions considered for the assessment are related to the analysis and design of Finite State Machine, the most complex topic of the course. Due to the Covid-19 pandemic and the disruption of the course's flow, results from Spring 2020, Fall 2020 and Spring 2021 were not included in the assessment, due to the change of format from in person to online. Results from the semesters affected by the pandemic are presented in Table 2 .

Question 5 asks students to draw a state diagram for an FSM being given specifications (statements). Students have to identify inputs, outputs, states, transitions, add an asynchronous reset, identify the number of required FFs.

"Design a MOORE FINITE STATE MACHINE for a Sequence Detector that detects —-consecutive bits of 0 in the input stream of bits, labeled ***y****. The output* ***z*** *is equal to 1 if during — consecutive clock cycles the input y was equal to 0. After the sequence is detected, the FSM returns to the initial state S0. Add an asynchronous Reset, active High to the FSM. How many FFs are required?"*

Question 6 asks students to implement a FSM using VHDL language being given the state diagram. Students are provided with different state diagrams such as soda dispenser, security systems, similar with lab and in-class examples.

"Write VHDL code for the following ——-controller, based on a synchronous FSM. What type of FSM is?"

Table 1. Students Final Exam Scores and Problem Scores

Academic Year/ Nr. of students	Final exam 100 points (min., max. grade)	Std. dev	Final exam question #5 15 points	Final exam question #6 15 points
Fall 2017/ Nr. of students=37	76.32 (min=0, max=99)	20.7	11.24	10.51
Spring 2018/ Nr. of students=24	81.04 (min=60, max=100)	13.00	11.25	11.94
Fall 2018/ Nr. of students=21	82.10 (min=54, max=97)	10.72	11.42	11.54
Spring 2019/ Nr. of students=21	82.09 (min=56, max=99)	11.46	11.95	11.50
Fall 2019 Nr. of students=30	82.32 (min=42, max=98)	12.91	11.33	11.96

For each semester, from Fall 2017 to Fall 2019, questions 5 and 6 were assessed to see if the goal for the course that 70% of the students meet the course assessment or not.

Figure 7 presents the results for problem 5 of the final exam. While in the academic year 2017-2018 the course assessment standard was not met (Fall 2017) or was partially met (Spring 2018). Starting in the academic year 2018-2019, the course assessment standard was met.

Figure 8 presents the results for problem 6 of the final exam. In the academic year 2017-2018 the course assessment standard was not met (Fall 2017). Starting spring 2018, the course assessment standard was met.

Possible explanations for the results are the emphasis on hands on-experiences during theory class and the focus on project assigned at the end of the semester. Using student feedback and the instructor's observations, the project specifications were revised from Fall 2018 to Spring 2019 by adding: 1) detailed specifications regarding the use of hardware resources on the FPGA board, 2) inclusion of the slow clock and 3) requirements for test benches. The project specifications were explained in great detail during theory sessions, not only labs.

Starting March 2020, all courses including labs were moved online. During Fall semester 2020, the EET 316 theory course was taught in a remote format while the laboratories were taught the hybrid format. During Spring semester 2021, the theory course and labs were all online in remote format. Adjustments were made every semester to accommodate the new formats, placing more emphasis on functional verification versus hardware implementation. Students' final exam scores from Spring 2020, Fall 2020 and spring 2021 are presented in Table 2. The exams were open notes, with books. No analysis or comparison with the previous semesters were performed. Every semester was slightly different and had various challenges due to the pandemic.

Starting Fall Semester 2018, student knowledge was assessed also from two lab experiments (lab 13 and 14), covering the Project Based Learning-Design and Implementation of a Vending

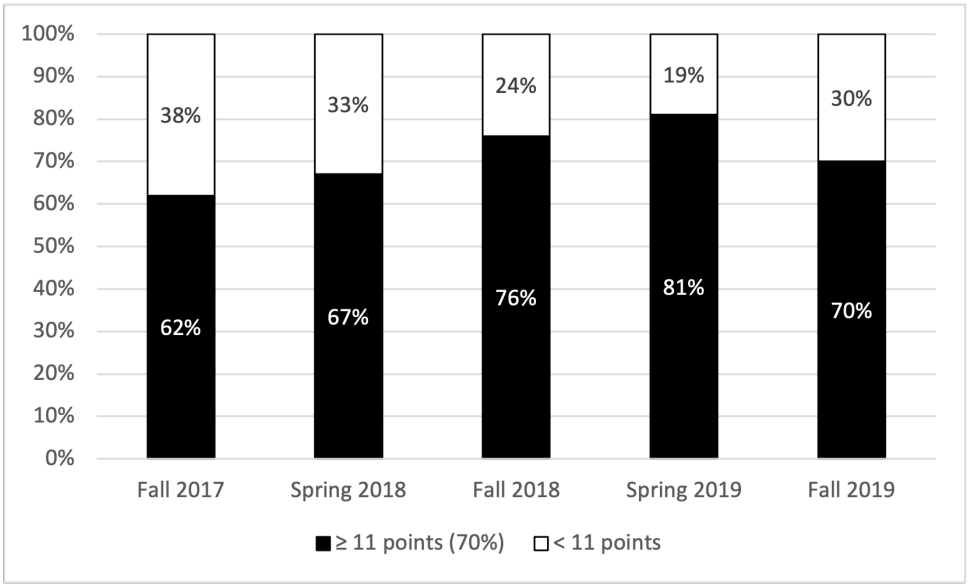

Figure 7. Problem 5 - Final Exam; Percentage of students with scores above and below 70%.

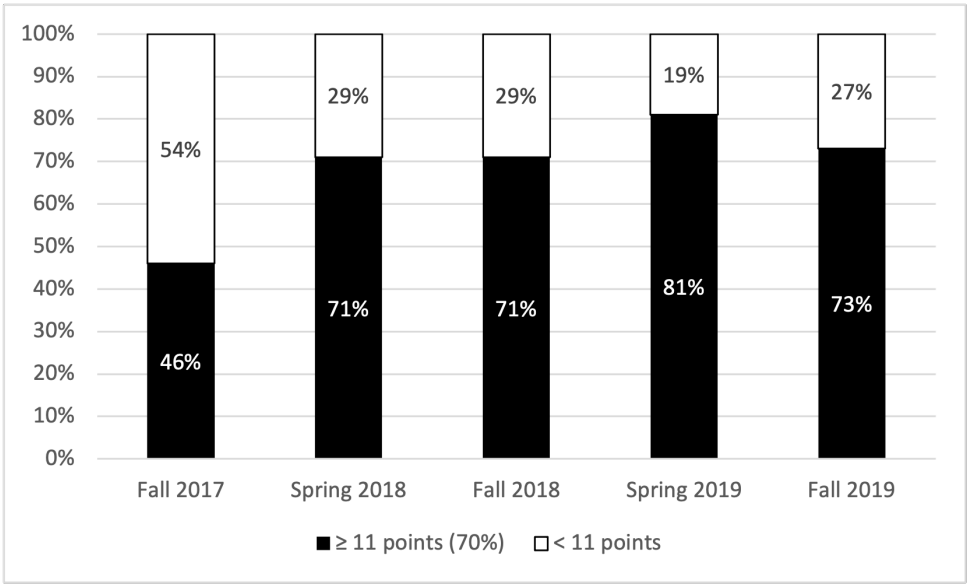

Figure 8. Problem 6 - Final Exam; Percentage of students with scores above and below 70%.

Table 2. Students Final Exam Scores- from Spring 2020 to Spring2021

Academic Year/ Nr. of students	Final exam 100 points (min, max. grade)	Std. dev final exam
Spring 2020/ 21 students	88.85 (65, 100)	11.78
Fall 2020/ 22 students	87.60 (64, 100)	11.28
Spring 2021/ 19 Students	87.5 (66, 100)	10. 22

Machine. The goal for the labs is that 70% of the students meet the assessment standard. An overall score over 84 % exceeds the standard, an overall score between 70 % and 84 % meets the standard, an overall score between 60% and 69% approaches the standard, while an overall score below 60 % does not meet the standard, according to ABET accreditation for the EET department.

The same group of students are enrolled in the lab and theory session during Spring semesters, allowing an easy flow of information from the theory to the lab sessions. In the Fall semesters theory and labs are covered by two different instructors, making synchronization of the FSM concepts and labs sometimes difficult. Regarding enrollment, twenty-six students were enrolled in two lab sections Fall 2018, twenty-one students were enrolled in one lab section Spring 2019, and thirty-two students were enrolled in two lab sections Fall 2019. Figure 9 and Figure 10 present the assessment results for PBL. The maximum score for project reports is 20 points, with 10 points possible for Design and 10 points possible for Functional Verification.

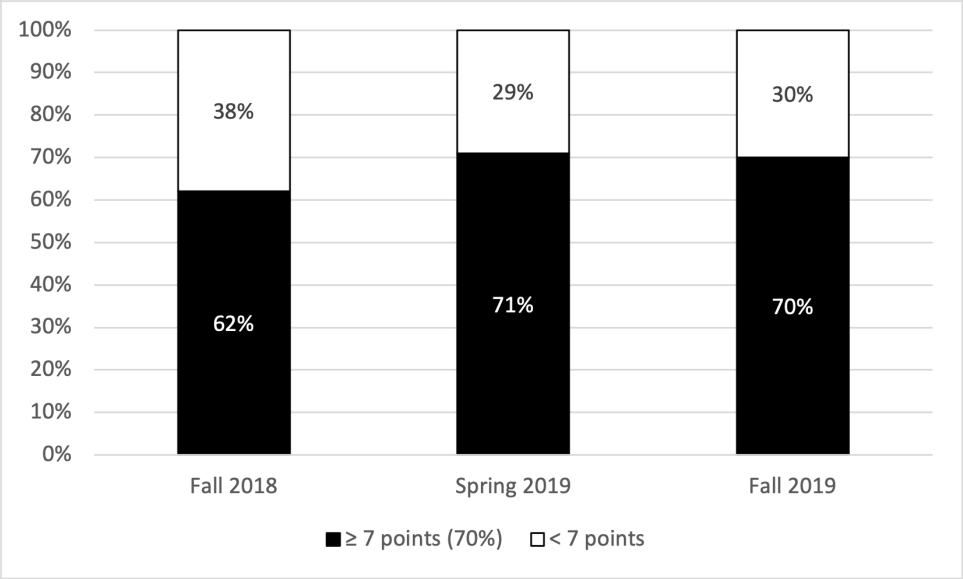

Figure 9. Project Based Learning - Part 1: Design and Implementation of a Vending Machine. Percentage of students with scores above and below 70%.

While in Fall 2018, the lab assessment standard was not met, starting in the Spring semester 2019, the lab assessment standard was met. Possible explanations for the results are the emphasis on hands on-experience (in class assignments) during theory class and the focus on project as presented in a previous paragraph. Holding the students responsible for finishing and demonstrating the project in a timely manner (no partial credit for incomplete project implementation or simulation) was an important goal to successful results.

Regarding students' performance in follow-up classes, it is important to mention that EET 316 is a prerequisite for EET 493-Design for Reliability and Testability of Digital Systems. The course is covered by the author of this paper every spring semester since 2017. The course is extremely well populated every academic year with an average of 18 students, minimum being 12 students to offer an elective course, and has presented good results. Due to the success of the current elective course, another elective course, EET 4xx-Testing and Testability of Digital Systems, will be offered in the next academic year.

As future work, the intention is to update the hardware to the next generation of Xilinx FPGA platforms and to Xilinx Vivado Design Suite. The complete set of active learning modules developed around the Analog Discovery will be offered Fall 2021, when courses and labs will be offered in person.

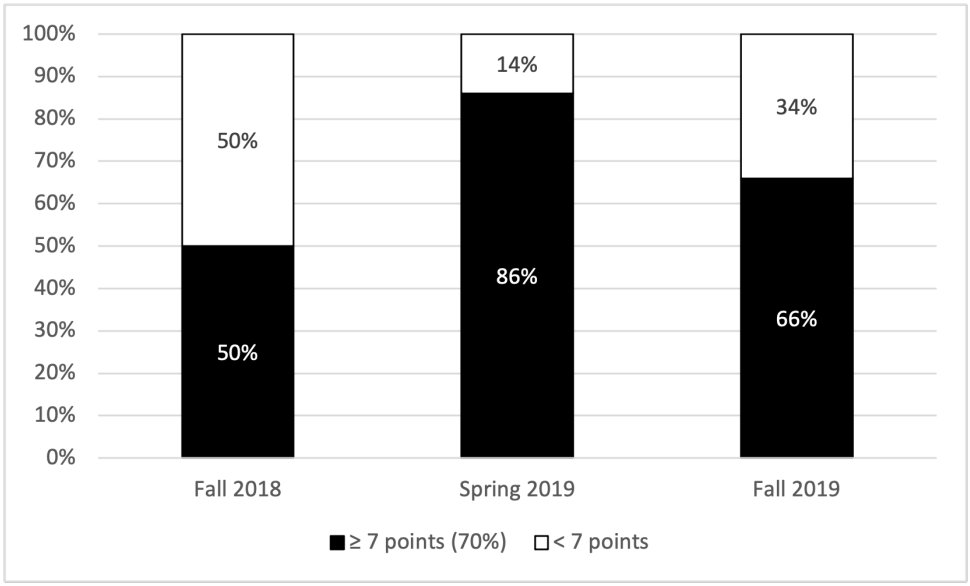

Figure 10. Project Based Learning - Part 2: Functional Verification of a Vending Machine. Percentage of students with scores above and below 70%.

7 Conclusions

The goal of this paper is to describe the motivation, methodology and results of applying active learning techniques in digital design education for engineering technology students. The active learning techniques incorporated in the Digital Design course and lab have the potential to improve students' engagement and learning in digital design. Engaging students to work on projects relating to real-world applications is a solid path to academic success. It has the potential benefit to help students to achieve a higher level of learning in the field of digital electronics and to develop essential employability skills. By giving students more opportunities to improve their employability skills, they will be better prepared to enter the competitive work force and to compete with graduates from other prestigious universities.

Acknowledgment

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Note: First results of the implementation of the flipped classroom pedagogy were presented at the ASEE 2019 national conference [21].

APPENDIX

Table 3. Tentative Course Schedule with Topics, Course Resources, Student Learning Outcomes (SLO) and Homework (HW).

Wk	Topic	Resources	SLO	HW
1	Introduction to Xilinx FPGA, Hardware Description Languages (HDLs), CAD Tools and Design Process Review: Digital Design Number systems	Course notes Ch. 1 ; 2	1,2	Hw 1
2	Combinational Logic Design: Logic gates, Boolean algebra, Boolean Functions and Equations, Truth Table Combinational logic optimization (K-maps)	Course notes Ch. 2.1-2.6, 2.8	1, 2	Hw 2
3	Combinational Logic Design: MSI logic circuits: Decoders, Encoders, Multiplexers, Code converters Adders, comparators, multipliers, subtractors	Course notes Ch. 2.9-2.10; 4.1, 4.3, 4.4, 4.6; 6.1-6.2	1,2	Hw3
4	Hardware Description Languages: Introduction to VHDL, Description of Combinational Logic Circuits using VHDL **MODULE 1-Flipped Classroom Video Tutorial** **EXAM 1**	Course notes Ch. 9.1 – 9.2. Optional: VHDL book	1,2	HW 4 Video Tutorial
5	Simulation (Functional Verification) and Test Benches for combinational circuits **MODULE 1-Flipped Classroom Video Tutorial**	Course notes Ch. 9.1 – 9.2.	2,3	Hw 5 Video Tutorial
6	Sequential Logic Design: Synchronous and Asynchronous Sequential Circuits, Clock Flip-Flops and Latches	Course notes Ch. 3.1, 3.2, 3.5	1,2,3	Hw 6
7	Registers, Shift Registers, Counters, Timers Impediments to Synchronous Design: Asynchronous Inputs, Clock Skew	Course notes Ch. 4.2, 4.8, 4.9 – 4.15	1,2,3	Hw 7
8	Description of Sequential Circuits in VHDL **MODULE 2-Flipped Classroom Video Tutorial**	Sec. 9.3 Optional: VHDL book:	1,2,3	Hw 8 Video Tutorial
9	Simulation (Functional Verification) and Test Benches for sequential circuits **MODULE 2-Flipped Classroom Video Tutorial**	Course notes Optional: VHDL book:	2,3	Hw 9 Video Tutorial
10	More Sequential and Combinational Logic description using VHDL Hierarchical Design **EXAM 2**	Course notes Optional VHDL book:	1,2,3	
11	Introduction to FSM (Finite State Machine). Controller design	Course notes Ch. 3.3-3.4	4	Hw 10
12	Mealy and Moore type FSM	Course notes Ch. 6.3	4	Hw 11
13	Description of Finite State Machine in VHDL **MODULE 3-Flipped Classroom Video Tutorial**	Course notes Optional VHDL book: Ch. 3	3,4	Hw 12 Video Tutorial
14	Simulation and Testbenches for FSM VHDL **MODULE 3-Flipped Classroom Video Tutorial** Review **EXAM 3** **FINAL EXAM**	Course notes	3,4	Video Tutorial

Table 4. EET 316- Laboratory Experiments

Wk	Lab Experiment
1	Introduction to CAD tool; Lab 1_AND Gate & Full Adder (Schematics)
2	Lab 2_ BCD to SSD Code Converter (Schematics)
3	Lab 3_ AND Gate & Full Adder (Introduction to VHDL)
4	Lab 4_BCD to SSD Code Converter (VHDL)
5	Lab 5_Functional Verification of Combinational _Circuits Test_Benches (VHDL)
6	Lab 6_Sequence Generator (Schematics)
7	Lab 7_Clock Divider (Schematics)
8	Lab 8_Fibonacci Series (Schematics)
9	Lab 9_ Clock-Divider-1Hz Clock (VHDL)
10	Lab 10_ Fibonacci (VHDL)
11	Lab 11_ Functional Verification of Sequential_ Circuits Test_Benches (VHDL)
12	Lab 12_ OneShot_FSM (VHDL) and Functional Verification of FSM
13	Project Design (VHDL)
14	Project Design (VHDL)

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