EXPERIENCING THE EFFECTS OF CLOCK TRANSITION TIMES ON CLOCKED STORAGE ELEMENTS

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Abstract

Designing synchronous sequential circuits consisting of clocked storage elements such as flip-flops needs to observe stringent setup time and hold time constraints. If there is a timing violation, meaning the input data changes within the setup time and hold time window of the active clock edge, the results of the clocked storage elements could be unpredictable, a situation called metastable state. The cause and symptoms of metastable state are well established in the digital design literature. However, the effects of clock transition times such as rise time and fall time on the behavior of a synchronous sequential circuit are rarely discussed.

This paper presents an experiment to demonstrate that the transition time of a clock signal can also affect the results of a clocked storage element. Understanding this effect is crucial for designing more robust complex high-speed digital systems consisting of clocked storage elements.

Introduction

A synchronous sequential circuit such as a Mealy or a Moore machine consists of three building blocks: the next state logic, the state variable storage, and the output logic. A single clock input controls the state transitions of a state machine. The state variable storage is implemented by a group of clocked storage elements such as flip-flops controlled by the clock signal. The state transition is determined by the output of the next state logic at the active clock edge, the rising-edge or the falling edge of the clock signal applied to the clocked storage elements.

A well-established design rule for interfacing with clocked storage elements is to observe the timing constraint: never change the data input to a flip-flop during the timing window of its setup time and hold time. Setup time is the time before the active clock edge and hold time is the time after the active clock edge. The timing analysis of a synchronous sequential circuit design is to make sure that the total propagation delay incurred by the next state logic and the storage elements plus the setup time is less than the clock cycle time.

A timing violation occurs when the data arriving at the input of a storage element does change during the setup time or the hold time. A timing violation can trap the storage element into a metastable state which generates invalid output voltage values for an unpredictable time interval with unpredictable final value. The end result is unpredictable synchronous sequential circuit behavior [1,2].

Design issues related to setup time and hold time have been widely discussed in the digital systems design literature, especially in the area of clock domain crossing in complex System-on-Chip designs [3]. However, effects of clock transition times such as the rise time and fall time are rarely mentioned in datasheets or in the literature. It is the purpose of this paper to provide this crucial information through three hands-on experiments.

These experiments use a 3-bit counter to demonstrate that a noisy slowly rising clock signal can affect the results of positive-edge triggered D flip-flops. The experiments clearly demonstrate that the higher speed of a D flip-flop, the more susceptible the D flip-flop is to slower clock transitions. Understanding the effect of clock transition times is therefore

crucial for designing robust synchronous sequential digital systems, especially for the systems consisting of high-speed clocked storage elements.

The paper is organized as follows. Section II presents a simple 3-bit counter design consisting of three positive-edge triggered D flip-flops. Section III discusses the experiment setup. Section IV details the experiment procedures. Section V summarizes the experiment.

A Synchronous 3-Bit Counter Design

A synchronous 3-bit counter can be designed by following the conventional sequential circuit design flow such as starting from the given task, drawing the state diagram, deriving its state table, generating the transition table, deriving its excitation table, and finally minimizing the excitation equations [2]. The minimized excitation equations for the three D flip-flops are:

$$D_0 = \overline{Q_0} \tag{1}$$
$$D_1 = Q_1 \oplus Q_0 \tag{2}$$
$$D_2 = Q_2 \oplus Q_1 Q_0 \tag{3}$$

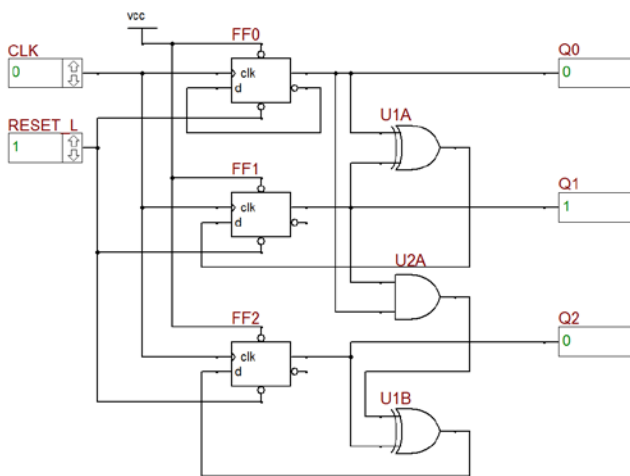The resulting synchronous 3-bit counter circuit diagram is shown in Figure 1.

Figure 1: The circuit diagram of a 3-bit synchronous counter.

Experiment Setup

The purpose of the experiment is to observe the effects of clock rise time on positive-edge triggered clocked storage elements such as the 74-series D flip-flops. To achieve this goal, a single-stepping clock generator consisting of a pushbutton switch needs to be constructed so that the 3-bit counter can be manually clocked by pressing the pushbutton switch. Each time the pushbutton switch is pressed to close its contacts, a rising clock edge is generated and the counter will increment by one. When the pushbutton switch is released to open its contacts, a falling clock edge is created. Each repetition of pressing and releasing of the pushbutton switch constitutes a clock cycle.

A. Switch debouncing

It is observed that the contacts of a mechanical switch bounce back and forth a few times before settling to their steady-state open or closed position, a phenomenon called switch bounce [2]. Thereby, simply pressing a pushbutton switch, its switch bounce can trigger multiple logic transitions in a digital circuit. To avoid generating such multiple logic transitions, a switch debouncer needs to be implemented.

B. Building a MAX6816-based single-stepping clock generator

The pushbutton switch can be debounced by a switch debouncer IC such as MAX6816 which changes its output state 40 ms after the input is stabilized [4]. A MAX6816-based single-stepping clock generator can be built as shown in Figure 2.
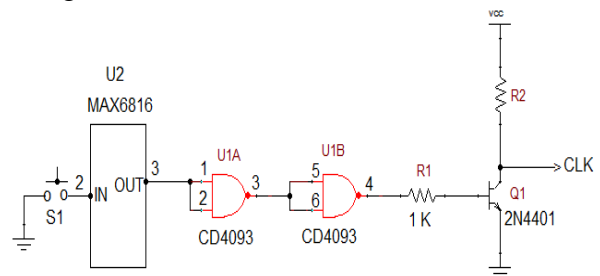

Figure 2: A single-stepping clock generator circuit based on a MAX6816 switch debouncer.

The debounced pushbutton switch then drives two cascaded CD4093 2-input NAND gates (or a single CD4081 2-input AND gate) and a 2N4401 transistor to provide a normally-LOW CLK output. The CMOS CD4093 is selected because it is used in the RC-based switch debouncer (as shown in Figure 3) and its high I_{OH} of -0.88 mA. The 2N4401 NPN transistor is mainly used for generating different rise times by changing its collector resistor, R2, value similar to designing a pull-up resistor for interfacing with an open-collector output. When R2 is greater than a certain value, i.e., when the clock rise time is longer than a certain value, the counter doesn't count correctly due to the excessive rise time.

C. Building an RC-based single-stepping clock generator

MAX6816 comes in a tiny SOT143 package and might cause difficulty in constructing the single-stepping clock generator. An alternative is to replace the MAX6816 by an RC-debouncer circuit [5] as shown in the left-half of Figure 3.
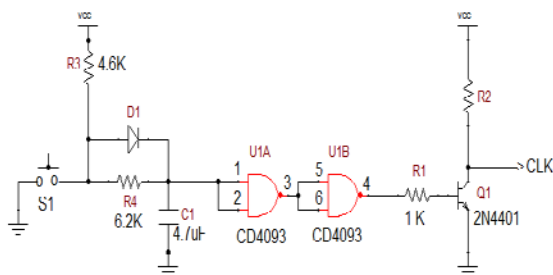

Figure 3: A single-stepping clock generator circuit based on an RC-debouncer.

At power-up, the pushbutton switch is open so capacitor C1 charges up toward Vcc - V_{D1} through R3 and D1 initially and then charges to Vcc through R3 and R4 when V_{C1} reaches Vcc - V_{D1}. When the pushbutton switch is pressed to close its contacts, capacitor C1 discharges to 0 V through R4. The Schmitt-trigger input of CD4093 has a specified minimum low-to-high threshold, V_T+, at 2.75 V and a maximum high-to-low threshold, V_T-, at 2.25 V. With Vcc = 5 V and V_{D1} = 0.3 V, R3 and R4 are calculated so that C1 will take at least 20 ms to discharge

from 5 V to 2.25 V through R4 when the switch is pressed and to charge from 0 V to 2.75 V through R3 and D1 when the switch is released.

This is assuming that the switch contacts will bounce for 20 ms every time the switch is pressed and released. The waveform captured at pin 1 of CD4093 (U1A) using a Tektronix MSO 2024 mixed-signal oscilloscope is shown in Figure 4. The waveform demonstrates how the RC-debouncer responds to the pressing and immediately releasing of the pushbutton switch.
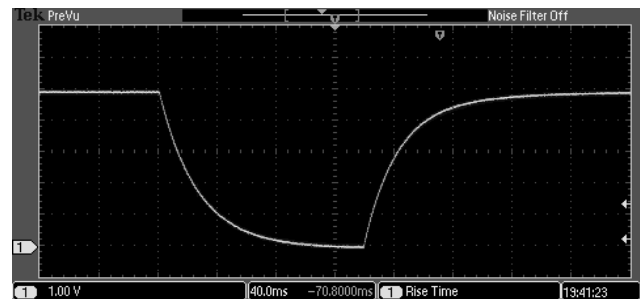

Figure 4: The RC-debouncer waveform.

The two CD4093 NAND gates and the 2N4401 NPN transistor (Q1) are mainly used to produce a normally-LOW clock signal for a normally-open pushbutton switch and, most importantly, for modifying the clock signal rise times. When S1 is open, C1 charges to 5 V, Q1 is on and CLK output is LOW. When S1 is pressed, C1 discharges to 0 V, Q1 is turned off, and CLK is HIGH. CLK goes LOW after S1 is released. Therefore, an active positive-edge is generated every time the pushbutton switch is pressed and the 3-bit counter should increment by 1.

D. Building the 3-bit counter

Build the 3-bit counter as shown in Figure 1 on a breadboard. The 3-bit counter is first implemented by using two 74LS74 chips for the three D flip-flops, a 74LS86 chip for the two Exclusive-OR gates, and a 74LS08 chip for the AND gate. Since the PR_L inputs of the three D flip-flops are not used, they are tied to Vcc. The three CLR_L inputs are connected to the RESET_L input which resets the 3-bit counter

to 000_2 when the RESET_L input is asserted to LOW. The clock inputs of the three D flip-flops are connected to the common clock input, CLK, which receives the rising clock edge from pressing the pushbutton switch, S1.

Experimenting with the Effects of Clock Transition Times

In digital systems, clock rise time can be increased due to increased loadings, excessively long signal paths, especially under overloaded condition when the output exceeds its fanout. It is very difficult to simulate the effect of rise time using a digital simulation software package, but can be easily observed by clocking the 3-bit counter using the single-stepping clock generator of Figure 2 or 3.

Experiment A: _Counter behaviors with proper clock rise time_

Connect the output (pin 3) of the first CD4093 NAND gate (U1A) to the 3-bit counter's CLK input. Pressing and releasing S1 will increase the counter by one and the counter will cycle through 000_2 to 111_2 correctly. The CLK waveform of 010_2 to 011_2 at pin 3 of U1A captured by a Tektronix MSO 2024 mixed-signal oscilloscope is shown in Figure 5. The CLK waveforms for other counter values are similar. The CLK waveforms all reach 2 V before 40 ns.
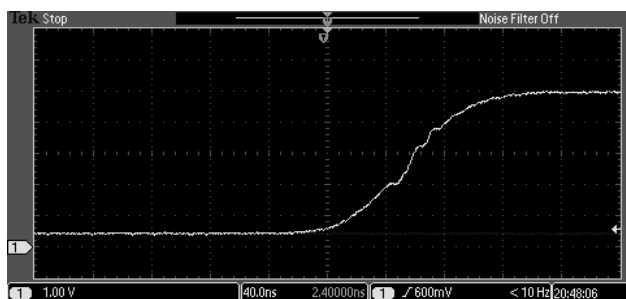

Figure 5: The clock waveform of counting from 010_2 to 011_2 observed at CD4093 pin 3.

In the tested counter circuit, the CLK signal goes through the same length from pin 3 of U1A to each D flip-flop's CLK input. Although the

CD4093 pin 3 is overloaded at output LOW with its $I_{OLmax} = 0.88$ mA driving three 74LS74 CLK input pins at I_{IL}max = -0.4 mA each and results in a raised output LOW voltage to about 0.4 V. However, its HIGH output is well within its fanout of $I_{OHmax} = -0.88$ mA driving three 74LS74 CLK input pins at I_{IH}max = 20 µA each. The CLK reaches 2 V around 40 ns. It is surprising to see that the CLK waveform is not a clean square waveform as shown in the timing diagrams generated by a simulation software package. With a timing scale of 40 ns/div, the CLK waveforms show similar variations when the 3-bit counter is going through different values.

Experiment B: _Counter behaviors with increased clock rise time_

This experiment is to observe the effects of rise time on the counter. First, remove the connection between CLK and CD4093 pin 3. Then connect the collector of Q1 to the CLK input and observe the behavior of the 3-bit counter with different R2 values. Larger R2 values tend to increase the clock rise times. From many experiments conducted by the author, it is observed that slower/older 74LS74 chips can tolerate larger R2 values up to 30 KΩ. Whereas, the counter built with newly purchased 74LS74 chips failed at R2 lower than 10 KΩ. Different 2N4401 transistors also showed different R2 values at which the counter started to fail. Therefore, the R2 values shown in the following steps need to be adjusted based on the age of the 74LS74 chips.

For a given R2 value as shown in the following steps, press the pushbutton switch multiple times and observe how the counter behaves. Also observe the CLK waveform using an oscilloscope if possible.

Step 1: R2 = 1 KΩ
Step 2: R2 = 5 KΩ
Step 3: R2 = 10 KΩ
Step 4: R2 = 20 KΩ
Step 5: R2 = 30 KΩ
Step 6: Swap 74LS74 chips and repeat step 5

The CLK waveforms counting from 010_2 to 011_2 at the collector of Q1 with different R2 values are shown in Figure 6. The waveform for R2 = 30 KΩ is very similar to R2 = 20 KΩ and is not included. The waveforms are captured by a Tektronix MSO 2024 mixed signal oscilloscope with a timing scale of 40 ns/div and voltage at 1 V/div. The waveforms show that the noise signals generated during digital logic transitions are superimposed on the CLK signal. As the R2 value increases, the CLK signal takes longer to reach 2 V and the voltage disturbances of the CLK signal become more pronounced before the CLK reaches 2 V.
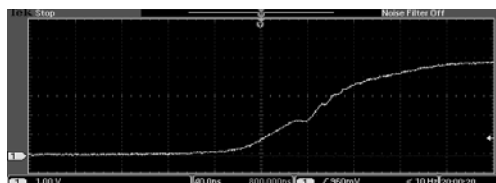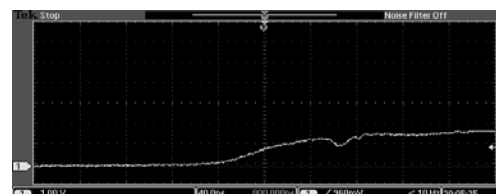

(a) R2 = 1 KΩ
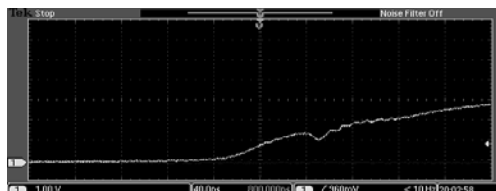
(b) R2 = 5 KΩ
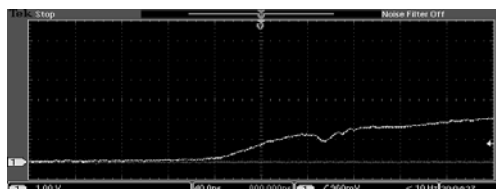
(c) R2 = 10 KΩ

(d) R2 = 20 KΩ

Figure 6: CLK waveforms for different R2 values when counting from 010_2 to 011_2.

The tested counter stuck at 110_2 and the capture waveforms are shown in Figure 7. Channel 4 is D0, Channel 3 is Q0, and Channel 1 is the CLK. These three waveforms illustrate how the counter got stuck at 110_2. When counter reaches 110_2, D0 is logic 1, therefore, Q0 should change to 1 after the next active clock edge. However, as Q0 changes to 1, D0 becomes 0, the voltage disturbance in the slow rising CLK triggers Q0 to change from 1 to 0.

The pronounced voltage disturbances on a slowly rising CLK signal could force the clock signal to oscillate around the active edge threshold voltage value multiple times before it passes through the Low-to-High logic transition region. This condition redefines the setup time and hold time region and easily results in a timing violation as demonstrated in Figure 7. Since D0 is directly obtained from $\overline{Q_0}$ of the 74LS74 chip without going through additional gates, the fast feedback can be viewed as a setup time violation when the CLK passes through the active edge threshold voltage value for the second time.
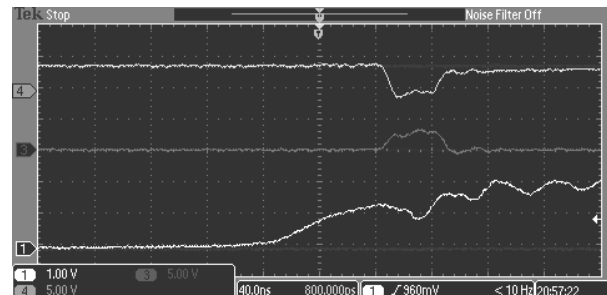

Figure 7: The waveforms show how the counter got stuck at 110_2 where Channel 4 is D0, Channel 3 is Q0 and Channel 1 is the CLK.

Experiment C: *Faster Logic requires more stringent clock timing*

To experiment the effects of rise time on faster logic, the components shown in Figure 1 can be replaced with 74F family components such as 74F74, 74F08, and 74F86. The 74F74 has much shorter typical propagation delays of t_{PLH} = 5.3 ns and t_{PHL}= 6.2 ns. Whereas, the 74LS74 has typical propagation delays of t_{PLH} = 25 ns and t_{PHL} = 30 ns.

Although the CD4093 pin 3 is overloaded at output LOW with its I_{OLmax} = 0.88 mA driving three 74F74 CLK input pins at I_{IL}max = -0.6 mA each, the captured CD4093 output LOW voltage is only showing around 0.2 V due to the much smaller actual 74F74 I_{IL} value. The CD4093 output HIGH output is well within its fanout of I_{OH} = -0.88 mA driving three 74F74 CLK input pins at I_{IH}max = 5 µA each. The CLK reaches 2 V around 40 ns. It is surprising to see that the CLK input signal is much noisier than when driving the 74LS74 chips. Figure 8 shows the CLK waveform when the counter is changing from 010_2 to 011_2.

The CLK is much cleaner when only one counter bit changes such as from 000_2 to 001_2, 010_2 to 011_2, etc. The CLK is noisier when two counter bits change values such as from 001_2 to 010_2, 101_2 to 110_2 etc. The CLK is very noisy when three counter bits change such as 011_2 to 100_2, except 111_2 to 000_2. These waveforms are repetitive at each test run.
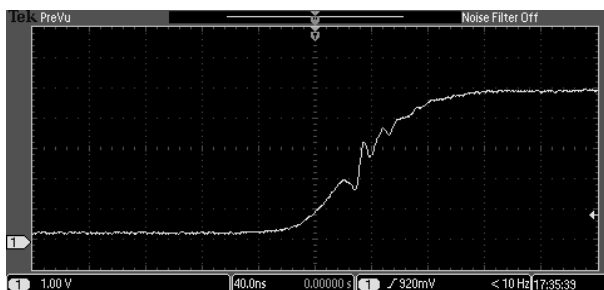

Figure 8: The clock waveform of counting from 010_2 to 011_2 observed at CD4093 pin 3.

This experiment is to observe the counter's behavior for different R2 values. For each R2 value shown in the following steps, observe how the counter behaves when the pushbutton switch is pressed each time. Also observe the CLK waveform using an oscilloscope if possible.

Step 1: R2 = 0.75 KΩ
Step 2: R2 = 1.5 KΩ
Step 3: R2 = 3 KΩ
Step 4: R2 = 5 KΩ
Step 5: Swap the 74F74 chips and repeat step 4.

The CLK waveforms counting from 010_2 to 011_2 at the collector of Q1 with different R2 values are shown in Figure 9. The waveforms are captured by the MSO 2024 at the time scale of 40 ns/div and 1 V/div. The tested counter failed at R2 = 3 KΩ when the counter began to skip 010_2 when it counts directly from 001_2 to 011_2.
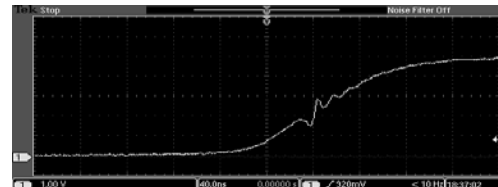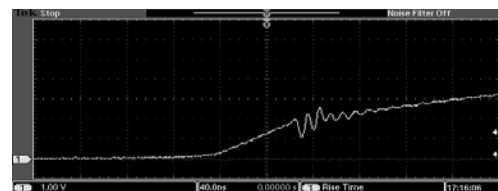

(a) R2 = 0.75 KΩ.
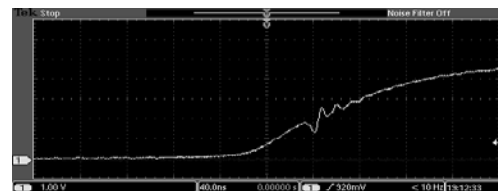
(b) R2 = 1.5 KΩ.
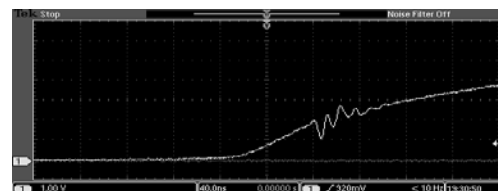
(c) R2 = 3 KΩ, 001_2 to 011_2 (skipping 010).

(d) R2 = 5KΩ, 001_2 to 011_2 (skipping 010).

Figure 9: CLK waveforms at different R2 values when counting from 010_2 to 011_2.

How the counter skipped 010_2 is illustrated in Figure 10. The top waveform is Q0 (Ch. 2) followed by Q1 (Ch. 3), Q2 (Ch. 4), and CLK (Ch. 1) at the bottom. When the counter is at 001_2, it should count up to 010_2 at the next active clock edge. The Q0 waveform shows it does go down to 0, but immediately bounces back to 1 within 20 ns and results in a very short 010_2 interval. This is due to the wiggling

voltage disturbances in the CLK signal oscillating around the clock active edge threshold voltage.

The 74F74 datasheet indicates the setup time and hold time should be at least 3 ns and 1 ns, respectively. The waveforms shown in Figure 10 can be interpreted as a hold time violation manifested as Q0's failure to hold on to its correct value.
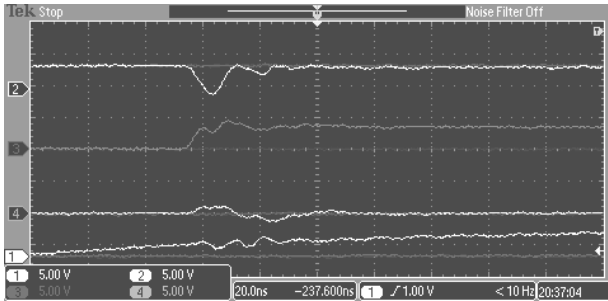

Figure 10: Waveforms showing how the counter jumps from 001_2 to 011_2.

Conclusion

The three hands-on experiments presented in this paper clearly demonstrate how an extended rise time of a clock signal could adversely affect the results of positive-edge triggered clocked storage elements. When the clock rise time is extended, the logic transition noises superimposed on a clock signal can cause the clock signal to oscillate around the clock edge threshold voltage value. This effect also occurs to extended fall time for negative-edge triggered storage elements.

Not only the oscillating clock voltage values can trigger a fast storage element to change its output state, the oscillating clock voltage values also can change the reference point of a clock edge for a clock cycle and result in setup time or hold time violations. The end result is a correct circuit design, but with a very frustrating partially working circuit prototype. The author was greatly puzzled by such symptoms before discovering that the extended clock transition time is the culprit.

Through many experiments using various types of 74-series clocked storage elements, it was observed that the faster the clocked storage elements, the more susceptible the storage elements are to the clock transition time. This finding serves as an important design guideline for high-speed digital systems design, especially for digital systems consisting of complex FPGA (field programmable gate array) or SoC (System-on-Chip) running at very high speeds.

In conclusion, this hands-on experience illustrates the potential adverse effect of clock transition times. Understanding this effect is crucial for designing robust synchronous digital systems consisting of high-speed clocked storage elements.

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